VIT Vidyalankar Institute of Technology
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TREILISIGN

cadence

Short Term Training Program (STTP)
Five Days (Offline Mode)

On

"CHIPCRAFT: Digital and Analog VLSI Chip Design using CADENCE"

(29th June 2026 to 3rd July 2026)

Convener
Dr. Akhil Masurkar
(In-Charge VLSI Design Lab)

Co-Convener
Dr. Arun Chavan (HOD-EXCS)
Dr. Girish Gidaye (HOD-EXTC)

Organized by:
Department of Electronics and Computer Science & Department of Electronics and Tele-Communication, Vidyalankar Institute of Technology, Vidyalankar College Marg, Wadala(E), Mumbai-400 037

About the CHIPCRAFT Workshop

The primary aim of the Short-Term Training Program (STTP) is to enhance the technical competency of faculty members and students in the domain of VLSI design using industry-standard Electronic Design Automation (EDA) tools. The program focuses on bridging the gap between theoretical knowledge and practical implementation by providing hands-on exposure to Cadence design tools. It is designed to equip participants with a comprehensive understanding of complete IC design flows, including full custom and semi-custom approaches.

The objectives of the STTP include improving teaching effectiveness through integration of advanced tools into the curriculum, strengthening research and development capabilities in VLSI design, and promoting industry-oriented skill development. The program also aims to facilitate the adoption of modern design methodologies aligned with current technological trends, thereby enhancing the employability and innovation capabilities of participants.

The training program is organized into focused modules that cover both Full Custom IC Design Flow and Semi-Custom IC Design Flow. Participants will gain hands-on experience in key stages such as schematic design, functional simulation, layout development, physical verification (DRC/LVS), parasitic extraction, and post-layout analysis. In addition, the semi-custom design module introduces advanced concepts including RTL synthesis, functional verification, design for testability (DFT), logical equivalence checking (LEC), physical implementation, timing analysis, and power optimization. These modules are demonstrated through practical case studies, enabling participants to relate theoretical concepts to real-world design scenarios.

Furthermore, the STTP includes post-installation training sessions conducted by industry experts, ensuring that participants receive guided instruction and practical exposure to the tools. In addition to immediate skill development, the STTP supports long-term academic enrichment by enabling institutions to integrate Cadence tools into curriculum delivery, laboratory experiments, and research activities. This initiative significantly contributes to capacity building in VLSI design and prepares participants for advanced research and industry applications.

Target Audience

Faculty, UG Students, PG students and Ph.D. Scholars from the AICTE approved institutions, Government, Industry and staff of host institute.

Registration

- **Last Date of registration 25th June 2026.**
- There shall be **No Registration Fees.**
- There are 50 seats. Selection is based on first-cum first serve basis.
- Shortlisted candidates will be announced through email within 2-3 days of online registration.
- Registration Link: https://forms.office.com/r/eeJfb2Umyi

QR for Registration

Vidyalankar Institute of Technology

Vidyalankar Institute of Technology (VIT) is an autonomous Engineering Degree and Management Institute, established in 1999, approved by AICTE and affiliated to the University of Mumbai. All Engineering programmes are accredited by the NBA. The Institute is accredited with A+ Grade by NAAC. The Institute strives to create industry-ready professionals and entrepreneurs by infusing the right blend of technological expertise and professional acumen and sensitizes them towards contributing to society.

About the Departments

The Department of Electronics and Computer Science, earlier known as Electronics Engineering at VIT was established in the year 1999. The Department of Electronics and Telecommunication was established in the Year 2006. Currently both the departments offer an undergraduate program with intake of 180 & 120 students respectively. The departments host well-equipped laboratories, and ICT-enabled teaching-learning processes that are supported by dynamic faculty with specialization in core competencies. The departments also actively conduct workshops, seminars, and faculty development programs (FDPs) to keep pace with evolving technologies. By bridging the gap between electronics and computing, they prepare students for careers in emerging tech domains while contributing to technological advancements in academia and industry.

Chief Patrons

Ms. Rashmi Deshpande, Chairperson, VDT

Mr. Vishwas Deshpande, Managing Trustee, VDT

Mr. Avinash Chatorikar, Secretary, VDT

Ms. Namrata Deshpande, Trustee, VDT

Mr. Milind Tadvalkar, Director, VDT

Patrons

Dr. Sangeeta Joshi, Principal, VIT

Dr. Saurabh Mehta, Chief Academic Officer, VIT

Convener

Dr. Akhil Masurkar (EXCS)

In-charge, VLSI Design Laboratory

Co-Convener

Dr. Arun Chavan (HOD-EXCS)

Dr. Girish Gidaye (HOD-EXTC)

Organizing Team

Technical Committee

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Dr. Anand Tripathi

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Prof. Anuradha Joshi

Prof. Faiz Rangari

Mr. Ajit Ghadge

Workshop Content

FULL CUSTOM DESIGN FLOW

- Introduction to Full Custom IC Design Flow
- Cadence Solutions for Custom IC Design
- Schematic Capture using Virtuoso Schematic Editor
- Symbol Creation
- Testbench Creation using Virtuoso Schematic Editor
- Functional Simulation using Spectre
- Layout Design using Virtuoso Layout Editor
- Physical Verification which includes DRC & LVS
- Parasitic Extraction using Quantus
- Post Layout Simulation
- Generation of GDSII

SEMI-CUSTOM DESIGN FLOW

- Introduction to Semi-Custom IC Design Flow
- Cadence Solutions for Semi-Custom IC Design
- Functional Verification using Incisive
- RTL Synthesis using Genus Synthesis Solution
- DFT (Design for Testability) using Modus
- LEC (Logical Equivalence Check) using Conformal
- Physical Implementation using Innovus that includes
  - ✓ Floor Planning
  - ✓ Power Planning
  - ✓ Placement
  - ✓ CTS
  - ✓ Routing
- Timing Analysis using Tempus
- Power Analysis using Voltus
- Parasitic Extraction
- Generation of GDSII

Eminent Speaker

Mr. Sanjay G S, Field Application Engineer at Entuple Technologies Pvt. Ltd., specializing in EDA tool deployment, hands-on training, and academic enablement using Cadence Design Systems.